Wide Input and Ultra-Low Quiescent Current Boost Converter with High Efficiency

General Description

The RT4823 is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery or two alkaline battery series, even when the battery voltage is below system minimum. The quiescent current in shutdown mode is less than 1μA, which maximizes battery life.

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Performance Specification Summary

The boost converter has an input voltage range from 1.8V to 5.5V, and the output voltage is 5V. It can operate in force bypass mode and boost mode. And the power-on inrush current and current limit are implemented serval setting for difference application. The RT4823 is available in a WL-CSP-9B 1.3x1.2 (BSC) package.

Table 1. RT4823WSC Evaluation Board Performance Specification Summary

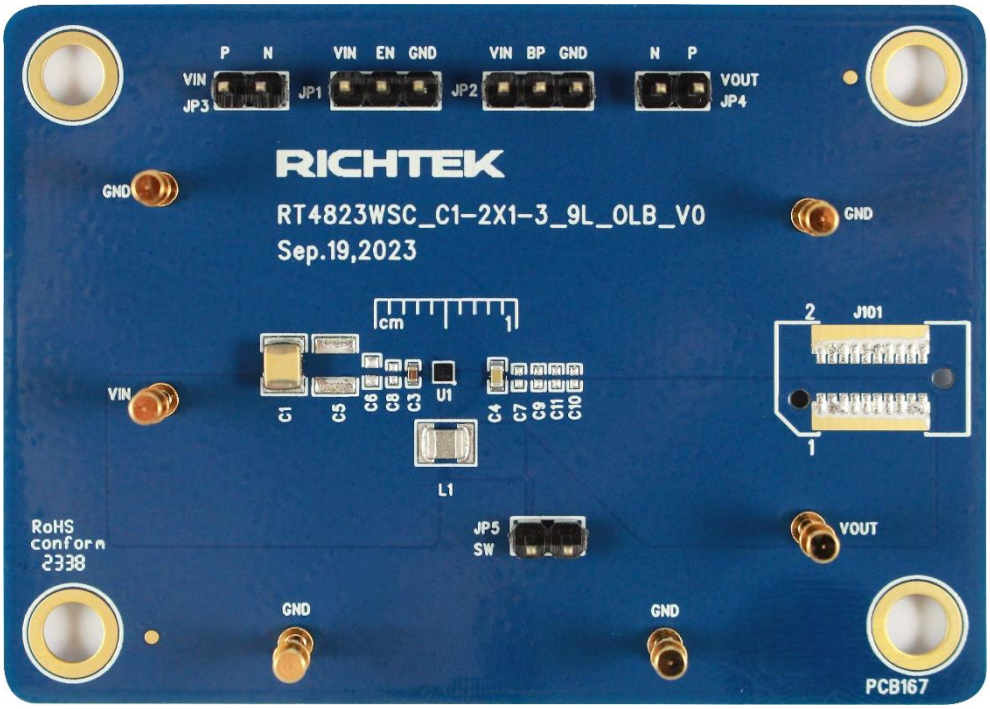
Specification	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range		1.8	--	5.5	V
Output Current	V_{IN} > 3V, V_{OUT} = 5V	0	--	1.3	A
Default Output Voltage		--	5	--	V
Operation Frequency		3	3.5	4	MHz
Output Ripple Voltage	V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 0.5A	--	40	--	mVp-p
Line Regulation	I_{OUT} = 0.5A, V_{IN} = 1.8V to 4.8V, V_{OUT} = 5V	--	±1	--	%
Load Regulation	V_{IN} = 3.6V, I_{OUT} = 0.2A to 1A, V_{OUT} = 5V	--	±1	--	%
Load Transient Response	V_{IN} = 3.6V, V_{OUT} = 5V ,I_{OUT} = 50mA to 500mA	--	±3	--	%
Maximum Efficiency	V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 0.6A	--	93	--	%

Power-up Procedure

1. Connect input voltage (1.8V < V_{IN} < 5.5V) to the VIN pin.
2. Bypass operation is set EN = Low, BP = High.
3. Boost operation is set EN = High, BP = Low.
4. To connect an external load to output and verify the output voltage versus applied current.

Detailed Description of Hardware

Headers Description and Placement



Carefully inspect all the components used in the EVB according to the following Bill of Materials table, and then make sure all the components are undamaged and correctly installed. If there is any missing or damaged component, which may occur during transportation, please contact our distributors or e-mail us at evb_service@richtek.com.

Test Points

The EVB is provided with the test points and pin names listed in the table below.

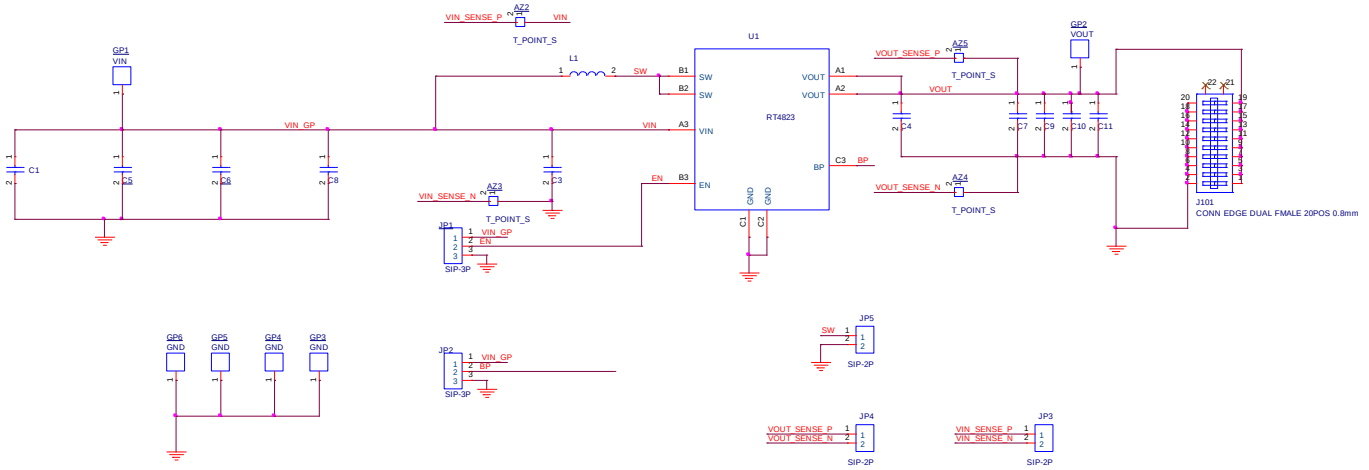
Test Point/ Pin Name	Function
VIN	Input voltage positive connection. The power supply must be connected to input connectors, VIN, and GND.
EN	Enable test point. The test point can be used to measure the enable signal.
VOUT	Output voltage connection. The load must be connected to output connectors, VOUT and GND.
JP1	EN jumper. Connect EN to ground to disable, connect EN to logic high to enable.
GND	Ground. Input/Output voltage return connection.
JP5	Switch node test point. The test point can be used to measure the switching node.
JP3	Input voltage sense point.
JP4	Output voltage sense point.
JP2	BP jumper. Connect BP to ground to disable, connect BP to logic high(and EN=Low) to enable bypass function.

Bill of Materials

Reference	Count	Part Number	Value	Description	Package	Manufacturer
C1	1	EMK325BJ476KM-T	47µF	Capacitor, Ceramic, 16V, X5R	1210	TAIYO YUDEN
C3	1	GRM155R60J475ME47D	4.7µF	Capacitor, Ceramic, 6.3V, X5R	0402	Murata
C4	1	GRM188R60J106ME47	10µF	Capacitor, Ceramic, 6.3V, X5R	0603	Murata
L1	1	DFE252012F-1R0M=P2	1.0µH/3.3A	Power Inductor	2.5x2.0x1.2mm	Murata
U1	1	RT4823WSC	RT4823	Step-Up DC-DC Converter	WL-CSP-9B 1.3x1.2 (BSC)	RICHTEK

Typical Applications

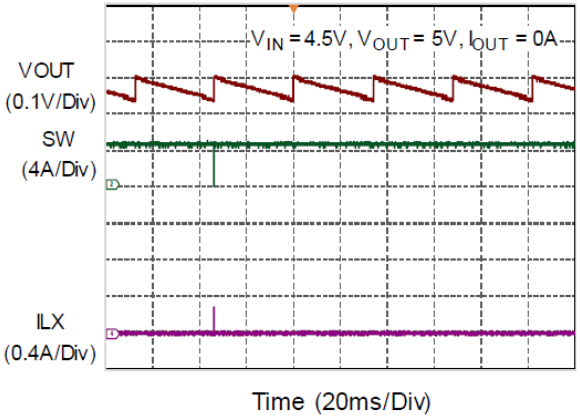
EVB Schematic Diagram



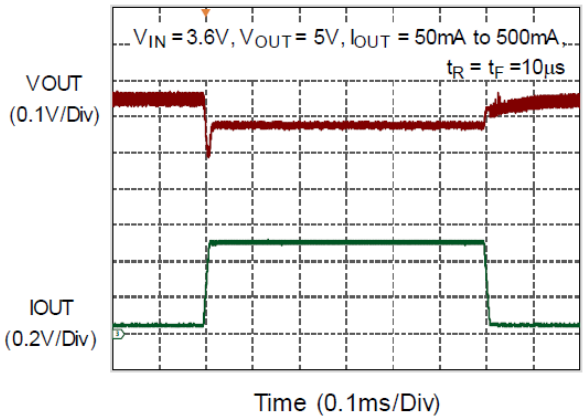
1. C1 is placed on input side, and the capacitors are design for long wire effect. If input source is close the RT4823 then the capacitors are optional.
2. C4 is placed on output side, and the capacitor is optional for output voltage ripple improvement.

Measure Result

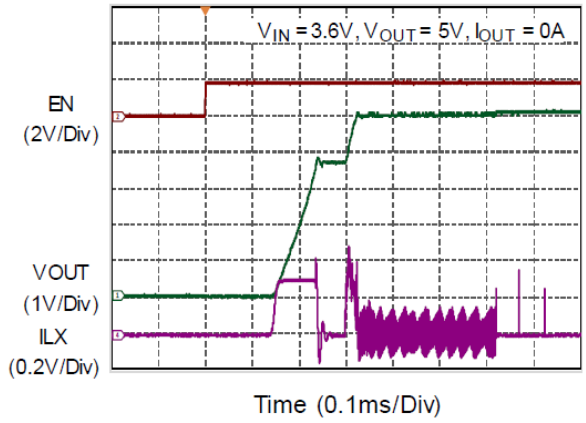
Output Ripple Measurement



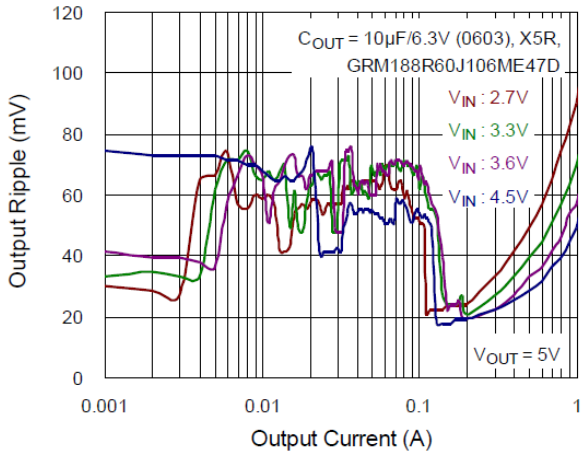
Load Transient Response



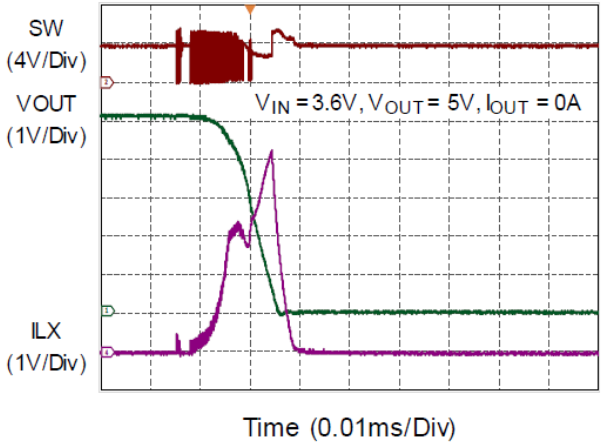
Power On from EN



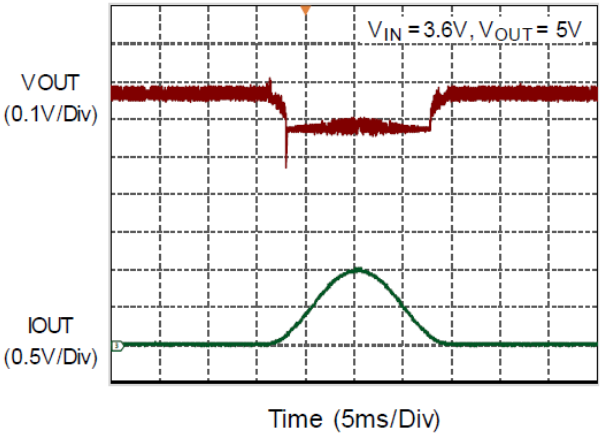
Output Ripple with Loading



Short Circuit Response



Sine Waveform Stability



Evaluation Board Layout

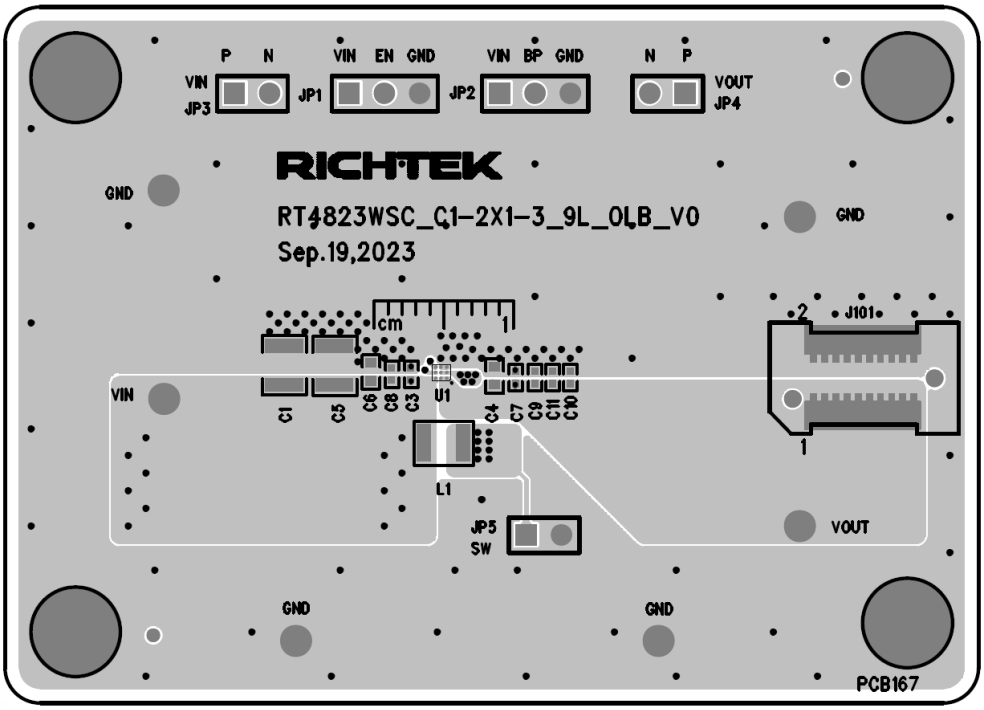


Figure 1. Top View (1st layer)

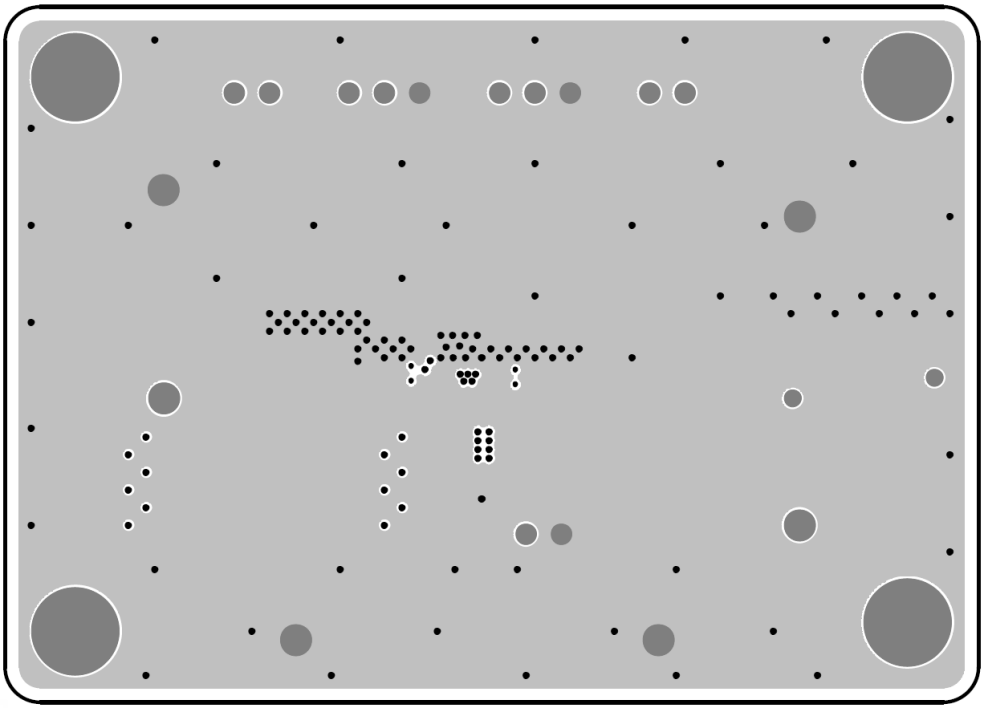


Figure 2. PCB Layout—Inner Side (2nd Layer)

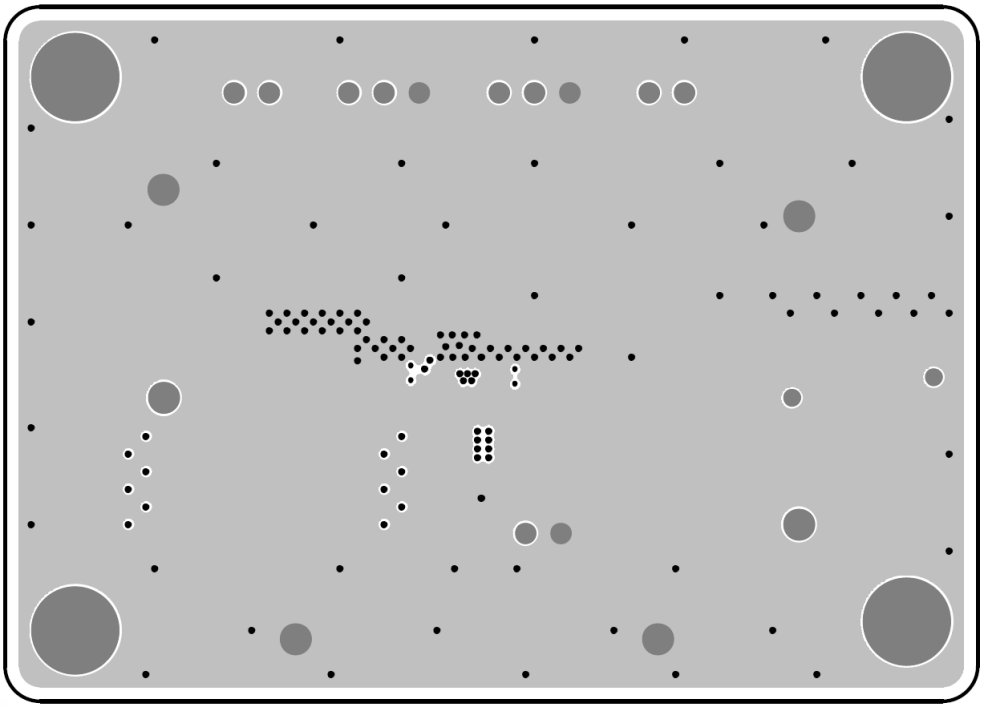


Figure 3. PCB Layout—Inner Side (3rd Layer)

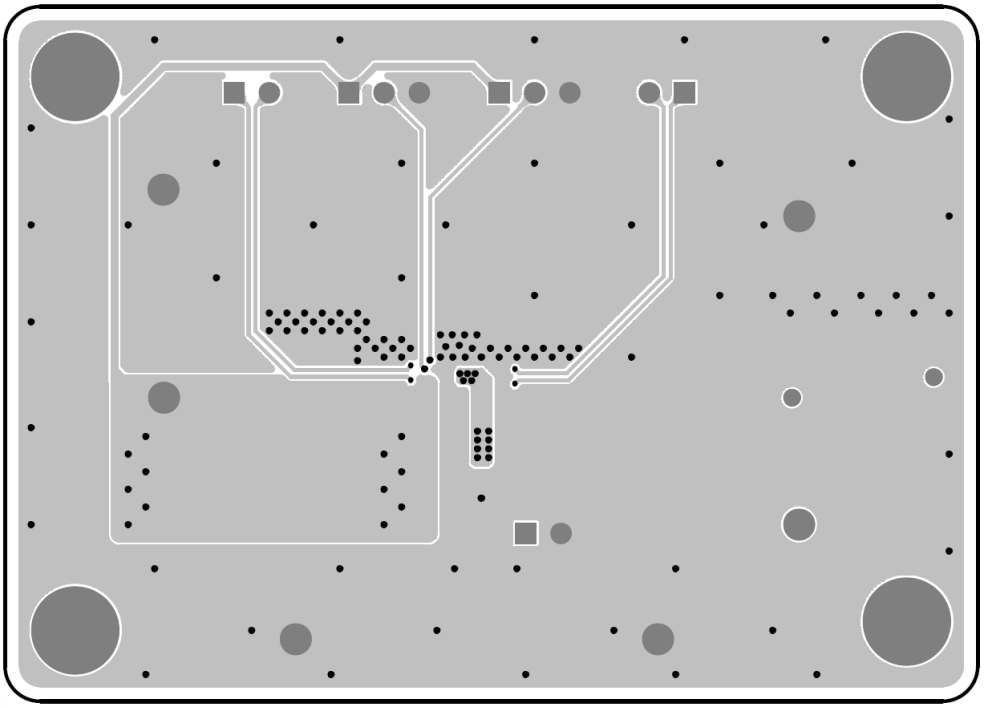


Figure 4. Bottom View (4th Layer)

More Information

For more information, please find the related datasheet or application notes from Richtek website http://www.richtek.com.

Important Notice for Richtek Evaluation Board